7001 High Density Switch System

SYSTEM

CAPACITY: 2 plug-in cards per mainframe.

MEMORY: Battery backed-up storage for 100 switch patterns.

SWITCH SETTLING TIME: Automatically selected by the mainframe for each card. Additional time from 0 to 99999.999 seconds can be added in 1ms increments.

TRIGGER SOURCES:

External Trigger (TTL-compatible, programmable edge, 600ns minimum pulse, rear panel BNC).

IEEE-488 bus (GET, *TRG)

Trigger Link

Manual (front panel)

Internal Timer, programmable from 1ms to 99999.999 seconds in 1ms increments.

STATUS OUTPUT: Channel Ready (TTL-compatible signal, rear panel BNC). Low going pulse (10µs typical) issued after relay settling time. For two different switch cards, 7001 will be set to the slowest relay settling time.

SWITCHING SEQUENCE: Automatic break-before-make.

MAINFRAME DIGITAL I/O: 4 open-collector outputs (30V maximum pull up voltage, 100mA maximum sink current, 10Ω output impedance), 1 TTL compatible input, 1 common.

RELAY DRIVE: 700mA maximum for both card slots.

CARD SIZE: 32mm high × 114mm wide × 272mm long (1¼ in × 4½ in × 10¾ in).

CARD COMPATIBILITY: Fully compatible with all 7XXX cards.

THROUGHPUT

EXECUTION SPEED OF SCAN LIST[1]

	7011 Card	7015 Card
Individual channels:	130/second	500/second
Memory setups:	125/second	450/second

TRIGGER EXECUTION TIME (maximum time from activation of Trigger Source to start of switch open or close[2]**):**

SOURCE	LATENCY	JITTER
GET[3]	200 µs	<50 µs
*TRG[3]	5.0 ms	
Trigger Link	200 µs	<13 µs
External	200 µs	<13 µs

1 Rates include switch settling time of cards: 3ms for 7011 and 500µs for 7015 cards.

2 Excluding switch settling time.

3 Assuming no IEEE-488 commands are pending execution.

IEEE-488 COMMAND EXECUTION TIME

	EXECUTION TIME[1]	
COMMAND	DISPLAY OFF	DISPLAY ON
OPEN (@1!1)	7.5 ms	8.5 ms
CLOS (@1!1)	7.5 ms	8.5 ms
MEM:REC M1	5.0 ms	6.0 ms

1 Measured from the time at which the command terminator is taken from the bus to the time at which the relay begins to open or close.

ANALOG BACKPLANE

SIGNALS: Four 3-pole rows (Hi, Lo, Guard). These signals provide matrix and multiplexer expansion between cards within one mainframe.

MAXIMUM VOLTAGE: 250V DC, 250V RMS, 350V AC peak, signal path to signal path or signal path to chassis.

MAXIMUM CURRENT: 1A peak.

PATH ISOLATION:

$>10^{10}\Omega$, <50pF path to path (any Hi, Lo, Guard to another Hi, Lo, Guard).

$>10^{10}\Omega$, <50pF differential (Hi to Lo or Hi, Lo to Guard).

$>10^{9}\Omega$, <75pF path to chassis.

CHANNEL CROSSTALK: <–65dB @ 1MHz (50Ω load).

BANDWIDTH: <3dB loss at 100MHz (50Ω load).

IEEE-488 BUS IMPLEMENTATION

STANDARDS CONFORMANCE: Conforms to SCPI-1990, IEEE-488.2 and IEEE-488.1.

MULTILINE COMMANDS: DCL, LLO, SDC, GET, GTL, UNT, UNL, SPE, SPD.

UNILINE COMMANDS: IFC, REN, EOI, SRQ, ATN.

INTERFACE FUNCTIONS: SH1, AH1,T5, TE0, L4, LE0, SR1, RL1, PP0, DC1, DT1, C0, E1.

GENERAL

DISPLAY: Dual-line vacuum fluorescent.

1st line: 20-character alphanumeric.

2nd line: 32-character alphanumeric.

REAR PANEL CONNECTORS:

IEEE-488

8-pin micro DIN connector for digital I/O

8-pin micro DIN for Trigger Link

8-pin micro DIN for Trigger Link expansion

BNC for External Trigger

BNC for Channel Ready

POWER: 100V to 240V RMS , 50/60 Hz, 50VA maximum.

EMC: Complies with to European Union Directive 89/336/EEC, EN61326-1.

SAFETY: Conforms to European Union Directive 73/23/EEC, EN61010-1.

EMI/RFI: Meets VDE 0871B and FCC Class B.

ENVIRONMENT:

Operating: 0°–50°C, <80% relative humidity (0°–35°C).

Storage: –25° to +65°C.

DIMENSIONS, WEIGHT: 89mm high × 216mm wide × 375mm deep (3½ in × 8½ in × 14¾ in). Net weight 3.4kg (7½ lbs).

Specifications subject to change without notice.